In the Claims: **Kindly amend Claims 21 and 22 as follows in the complete listing of claims. No new matter has been introduced.**

1. (withdrawn) A via etching process for a polymer layer deposited on a semiconductor substrate comprising said steps of:
placing a hard-mask on said polymer layer;
placing a photoresist mask on said hard-mask;
releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining said via hole; and
releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with vertical sidewalls.

2. (withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises
trifluoromethane and argon.

3. (withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

4. (withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

5. (withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts.

6. (withdrawn) A via etching process as recited in Claim 1, wherein said said step of releasing first fluoride gas further includes for approximately three to seven minutes doing all the following: applying a first fluoride gas comprising an equal ratio of

trifluoromethane and argon, applying a pressure of approximately 10 milli-Torr, applying a temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts, and applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

7. (withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen.

8. (withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen, wherein said volume ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen.

9. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer etching step further comprises applying bias power within the range of approximately 57 Watts to approximately 62 Watts.

10. (withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 475 Watts to approximately 505 Watts.

11. (withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes for approximately one and half minutes to six minutes doing all the following: applying a second fluoride gas comprising Sulfur Hexafluoride and Oxygen, wherein said ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen with an associated pressure of approximately 5 milli-Torr, applying temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power with the range of approximately 475 Watts to approximately 505 Watts, and applying bias power comprising a bias power with the range of approximately 25 Watts to approximately 32 Watts.

12. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is benzocyclobutene polymer.

13. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is a material with a dielectric constant less than 3.

14. (withdrawn) An etch process as recited in Claim1, wherein said semiconductor substrate is chosen from the group consisting of Indium Phosphide and Gallium Arsenide.

15. (withdrawn) A via etching process for a polymer layer on a semiconductor substrate comprising the steps of:

placing in a chamber said semiconductor substrate including a polymer layer defining a sub-micron wide via-opening deposited on said semiconductor substrate, and a hard-mask defining said sub-micron wide via-opening deposited on said polymer layer;

releasing a third fluoride gas into said chamber;

applying bias power within the range of approximately 105 Watts to approximately 120 Watts;

applying pulse-modulated power within the range of approximately 725 Watts to approximately 755 Watts;

pressurizing said third fluoride gas within a range of approximately 5 milli-Torr to approximately 20 milli-Torr; and

continuing the above steps until etching said hard-mark and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening creating tapered sidewalls.

16. (withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride gas comprises trifluoromethane and argon.

17. (withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

18. (withdrawn) A via etching process as recited in Claim 15, wherein said continuing the above steps within the range of approximately three minutes to approximately seven minutes.

19. (withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is benzocyclobutene polymer.

20. (withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is a material with a dielectric constant less than 3 and has an etch rate 10 times slower than that of said hard-mask layer.

21. (currently amended) A device including a via produced by the process comprising the steps of:

placing a hard-mask on ~~said~~ a polymer layer;

placing a photoresist mask on said hard-mask;

releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining ~~said~~ a via hole; and

releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical ~~sidewalls~~ sidewall, whereby the via hole comprises an aspect ratio which is greater than 1.

22. (currently amended) A device including a via produced by the process comprising the steps of:

placing, in a chamber, ~~said~~ a semiconductor substrate including a polymer layer defining a sub[[-]]micron wide via-opening deposited on said semiconductor substrate, and a hard-mask defining said sub[[-]]micron wide via-opening deposited on said polymer layer;

releasing a third fluoride gas into said chamber;

applying bias power within the range of approximately 105 Watts to approximately 120 Watts;

applying pulse-modulated power within the range of approximately 725 Watts to approximately 755 Watts;

pressurizing said third fluoride gas within a range of approximately 5 milli[[-]]Torr to approximately 20 milli[[-]]Torr; and

continuing the above steps until etching said hard-mark and an exposed portion of said polymer layer proximal to said sub[[-]]micron wide via-opening thereby creating at least one tapered ~~sidewalls~~ sidewall, whereby the via opening comprises an aspect ratio which is greater than 1.